

Amendments to the Claims

1. (CURRENTLY AMENDED) A semiconductor device having opposed first and second major surfaces, comprising:
 - a body region ~~(4)~~ at the first major surface;
 - at least one cell ~~(18)~~ having longitudinally spaced source and drain implantations ~~(22, 24)~~ extending into the body region ~~(4)~~ from the first major surface, the source and drain implantations ~~(22, 24)~~ being spaced away from the substrate ~~(2)~~ by part of the body region ~~(4)~~ and defining a channel part ~~(40)~~ of the body region ~~(4)~~ between the source and drain implantations; and
 - at least one insulated gate trench ~~(42)~~ extending longitudinally from the source implantation ~~(22)~~ to the drain implantation ~~(24)~~ through the body region ~~(40)~~, the insulated gate trench ~~(42)~~ including a gate conductor ~~(50)~~ insulated from the source and drain implantations ~~(22, 24)~~ and the body region ~~(40)~~ by a gate dielectric ~~(44, 46, 48, 64, 66)~~ along the side and end walls and the base of the trench, the source and drain implantations extending along part of the side walls of the trench,
 - wherein the source and drain implantations ~~(22, 24)~~ include conductive shallow contact regions ~~(26, 28)~~ at the first major surface, extending vertically into the body to a depth of no more than 35% the depth of the trench.
2. (ORIGINAL) A semiconductor device according to claim 1 wherein the body region is of first conductivity type and the shallow contact regions are of a second conductivity type opposite to the first conductivity type.
3. (CURRENTLY AMENDED) A semiconductor device according to claim 1 or 2 wherein each of the source and drain implantations ~~(22, 24)~~ further comprises a lower doped region ~~(30, 32)~~ of lower doping than the shallow contact region.
4. (CURRENTLY AMENDED) A semiconductor device according to claim 3, wherein:

the source implantation ~~(22)~~ includes a higher doped shallow source contact region ~~(26)~~ and a lower doped source drift region (30) between the higher doped source contact region ~~(26)~~ and the body ~~(40)~~;

the drain implantation ~~(24)~~ includes a higher doped shallow drain contact region ~~(28)~~ and a lower doped drain drift region ~~(32)~~ between the higher doped drain contact region ~~(28)~~ and the body ~~(40)~~;

the insulated gate trench ~~(42)~~ includes potential plate regions ~~(60)~~ extending longitudinally on either side of a central region ~~(62)~~, the potential plate regions ~~(60)~~ being adjacent to the source and drain drift regions respectively, and the central region ~~(62)~~ being adjacent to the body; and

the thickness of the gate dielectric sidewalls ~~(64,66)~~ of the insulated gate trench ~~(42)~~ is greater in the potential plate regions ~~(60)~~ of the insulated gate than the central region ~~(62)~~.

5. (CURRENTLY AMENDED) A semiconductor device according to ~~any preceding claim~~ claim 1 comprising a plurality of cells ~~(18)~~ laterally spaced across the first major surface.

6. (CURRENTLY AMENDED) A semiconductor device according to claim 5 wherein gate trenches ~~(42)~~ alternate with Creeils ~~(18)~~ laterally across the surface.

7. A semiconductor device according to claim 5 wherein each cell ~~(18)~~ has a gate trench ~~(42)~~ laterally within the confines of the cell.

8. (CURRENTLY AMENDED) A semiconductor device according to claim 3 wherein the lower doped region ~~(30,32)~~ of lower doping than the shallow contact region extends vertically below the shallow contact region ~~(26,28)~~ to a depth at least 80% of the depth of the trench.

9. (CURRENTLY AMENDED) A semiconductor device according to ~~claim 1 or 2~~ claim 1, wherein the source and drain implantations ~~(22, 24)~~ consist exclusively of the shallow contact region ~~(26, 28)~~.

10. (CURRENTLY AMENDED) A semiconductor device according to any
~~preceding claim~~claim 1 on a conductive substrate ~~(2)~~ of first conductivity type.